A 94-GHz Planar Monopulse Receiver

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Abstract— **This letter presents the first results on a 94-GHz integrated monopulse receiver. The receiver is based on a 23-GHz local oscillator driving four separate phase-coherent 94-GHz subharmonic mixers, and performs monopulse processing on the IF signals. All circuits are integrated on a single wafer, and are realized using uniplanar coplanar-waveguide (CPW), slot lines and coplanar striplines (CPS). These features result in a compact, low-cost system suitable for tracking systems operating in poor visibility conditions, as well as in collision avoidance receivers for automotive applications.**

I. Introduction

RECENT advances in millimeter-wave planar antennas and circuits have spurred research in the development of novel integrated subsystems with improved performance and lower fabrication costs [1], [2]. One such system, an integrated four-horn monopulse tracking receiver, has been designed and fabricated for operation at 94 GHz. The receiver is integrated on a single high-resistivity silicon chip, and is composed of uniplanar CPW, slotline and CPS circuits. This eliminates the need for a backing ground-plane and precision via-hole placement when utilizing three-terminal devices in the system. The uniplanar design is compatible with planar dipole and slot antennas [3].

II. Circuit Description

The receiver consists of four antennas in a 2 x 2 array to generate the normalized sum and difference patterns. An anti-parallel Schottky diode pair is placed at the feed of each antenna to form a 94-GHz subharmonic mixer, and is driven by an on-chip 23-GHz local oscillator (LO). Fig. 1 shows the receiver layout. The circuits are integrated on a high-resistivity silicon or gallium arsenide substrate, and all the semiconductor devices are commercially available and hybrid-mounted. Wire bonds are used to equalize the CPW ground planes. The integrated antennas consist of planar dipoles on sections of 0.1 λ_d-thick silicon (or GaAs) suspended inside integrated horn cavities [4]. The 0.1 λ_d-thick substrate located beneath each dipole is obtained by etching the silicon (or GaAs) behind the antenna until 90 μm of material remains. Grooves at the edges of this slab are completely etched through to produce trenches necessary to prevent power loss to substrate modes. The placement of these trenches need not be precise. The integrated horn cavity increases the directivity of the dipole from about 6 dB to 13 dB. The LO power is injected into the mixers using coplanar stripline (CPS), which is best suited to feed the dipoles. A capacitive overlay on the CPS isolates the 94-GHz RF power from the 23-GHz LO and 200-MHz IF circuitry. The CPW transitions to CPS using a CPW-slotline-CPS balun, which also distributes the power among mixers. The dipole antenna presents a reactive impedance at 23 GHz, and thus does not radiate the LO power. The 200-MHz IF signal is extracted from the antenna by inserting a break in the slotline. A capacitive overlay across the break presents a short circuit at 23 GHz and an open circuit at 200 MHz, thereby keeping the LO and IF circuits isolated. The individual IF signals from each of the four horns are fed into IF amplifiers and a monopulse processor to obtain the sum and difference patterns.

III. Design and Measurements

Harmonic balance analysis simulation was used to predict the performance of subharmonic mixers based on commercially available diodes. The antiparallel Schottky diodes used in the mixer are MA/COM MA40 422 with a C_{j0} of 50–70 fF per diode, $R_s = 3\ \Omega$, $L_s = 0.1$ nH and $n \leq 1.1$. Because of the relatively large C_{j0}, the optimum RF impedance is about 15 Ω, calculated from harmonic balance analysis (HBA) [5]. The dimensions and location (within the horn cavity) of the planar dipole antenna were empirically optimized using microwave scale model measurements. These efforts produced an antenna design consisting of a 970-μm long, 220-μm wide dipole on a 0.1 λ_d (90-μm thick) substrate located 0.36 λ from the apex of the cavity. This structure has an input impedance of 16Ω at 94 GHz and reactive impedances at the other harmonics of 23 GHz, providing a good RF match and embedding impedances for the antiparallel diodes when they are being pumped with sufficient LO power.

The VCO circuit is fabricated using the NEC NE32100 HEMT connected in a common gate configuration, and is designed using a reflection amplifier approach [6]. Two varactors with $C_{j0} = 0.6$ pF are attached at the gate for frequency tuning. The measured output power from the VCO is approximately 1 ± 0.5 mW. The tuning range for a 0–15 V varactor bias was measured to be over 200 MHz with a 3-dB power variation.

The power needed to drive each subharmonic mixer is about 8 mW. Losses at 23 GHz in a 50-Ω CPW line and the 10 pF ac-coupling capacitors were measured to be 0.8 dB per guided wavelength λ_g and 0.4dB, respectively. Measurements were performed on a DC-40GHz probe station. Therefore total loss from transmission lines, transitions, capacitors, and mismatch to the anti-parallel diodes are estimated to be approximately 6 dB. An amplifier chain with at least 20 dB of gain and the

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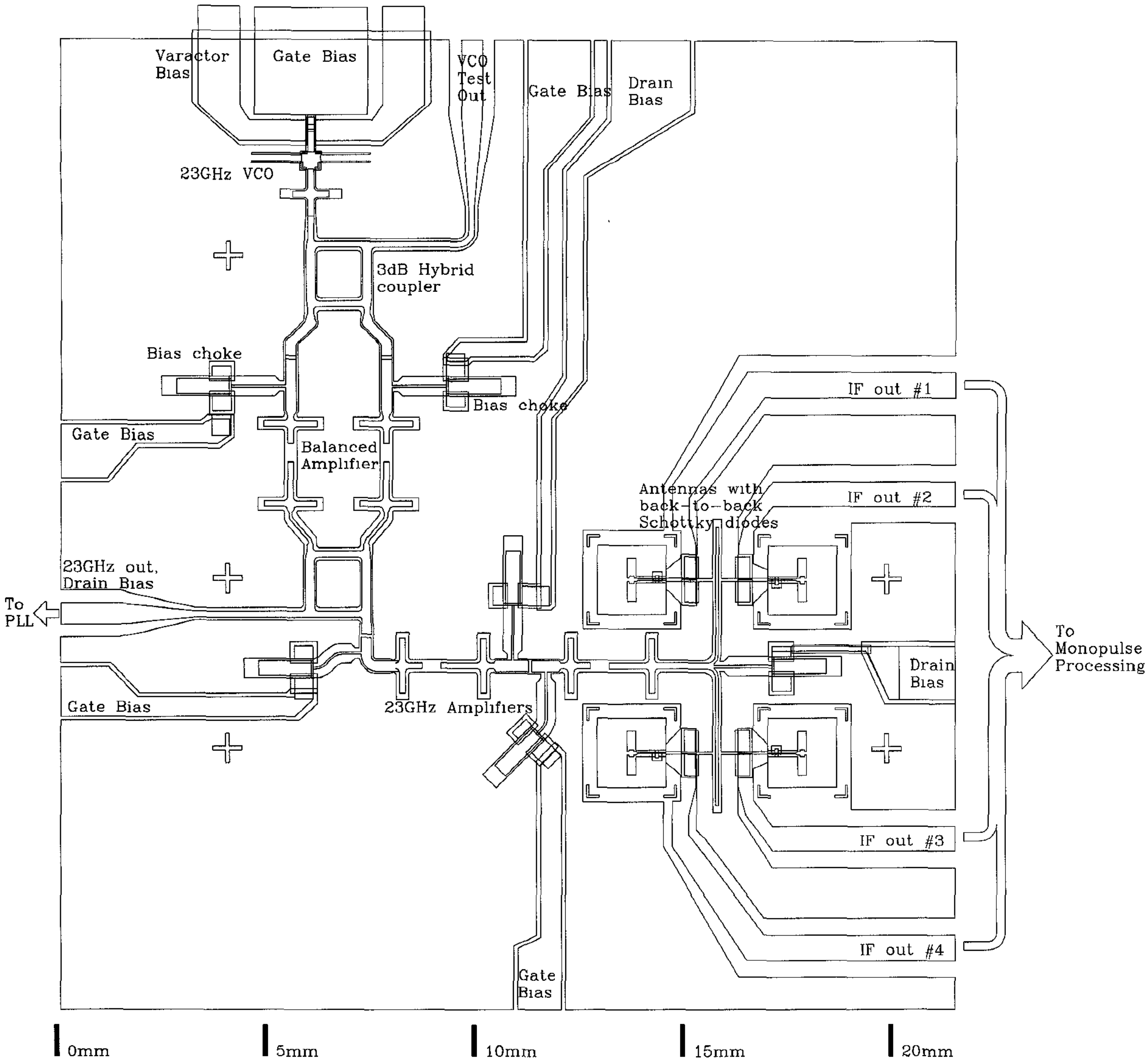

Fig. 1. The 94GHz planar subharmonic monopulse receiver design.

ability to handle 60 mW is required. The first stage of the chain consists of a balanced amplifier with very good input/output matching and stability. The Fujitsu FLR016XV transistors are used and are capable of handling more than 60 mW at 23 GHz. The individual amplifier designs were measured from 20 to 26GHz using on-wafer probing and TRL calibration techniques. However, the combined gain of the three stages was not measured. Measured S-parameter data yielded close agreement with calculations, and the gain of the individual stages was between 6 and 7 dB. The total designed gain of the three stages is 20 dB.

The measured radiation patterns the 94 GHz monopulse receiver are shown in Fig. 2. These patterns are synthesized using a 200-MHz IF monopulse processor. The relative phase data shown in Fig. 2 (b) is the data taken directly from phase discriminators in the IF monopulse processor. The null in the E and H planes is lower than 30 dB and is limited by the dynamic range of instrumentation. The sum pattern sidelobes are −10 dB and are a result of the 1.5 λ spacing between adjacent array elements. Measured cross polarization was below 20 dB. A conversion loss (defined as the measured IF power divided by the RF power available at the dipole apex) of 20 dB was measured for a 23.5-GHz LO. This is about 6dB higher than the predicted value using harmonic balance analysis, and is most likely due to insufficient LO power. It should also be noted that the MA/COM 40422 antiparallel diodes are designed to be used at K-band frequencies. They were selected because they are the highest-frequency antiparallel Schottky diodes commercially available. The monopulse chip has been used successfully in laboratory tests to track a source over a ±25° range in the elevation and azimuth directions.

IV. Conclusion

A 94-GHz integrated monopulse tracking receiver has been developed using uniplanar circuits and antennas. The receiver uses subharmonic mixers with on-chip local oscillators to achieve a compact, rugged and low-cost design. The design is compatible with other planar antennas, such as CPW-fed slots or aperture-coupled microstrip antennas. The chip area can be reduced by a factor of at least two in future designs, and

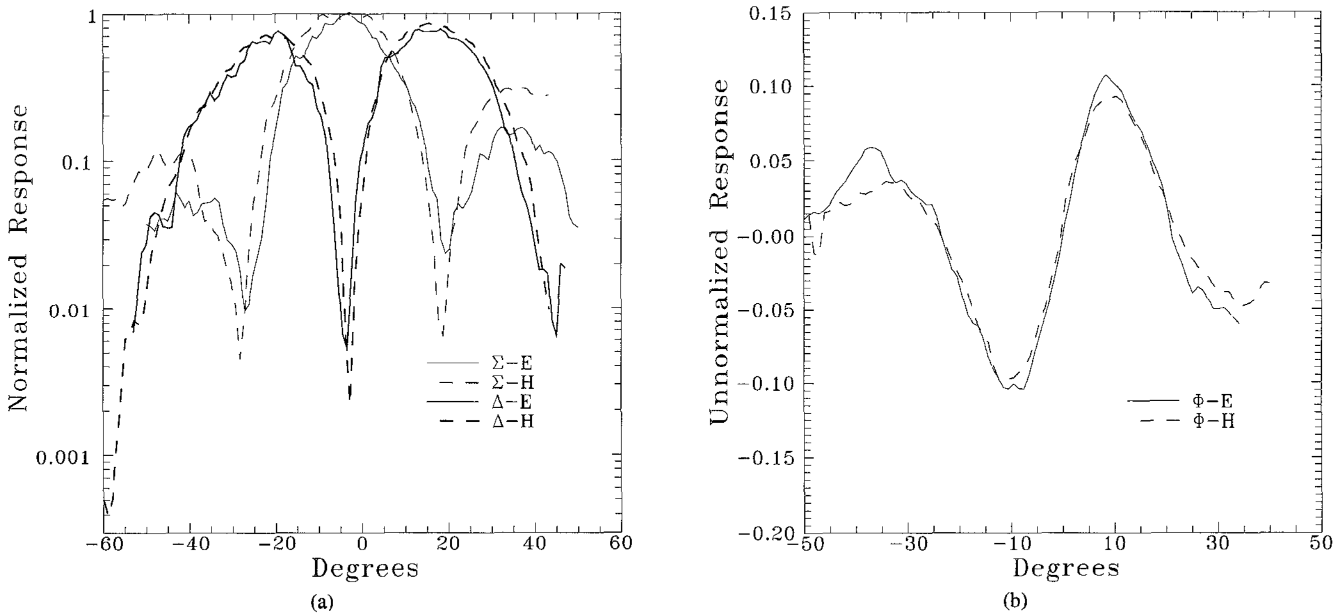

Fig. 2. Measured sum and difference monopulse patterns for E and H planes. Normalized amplitude (a) and relative phase (b).

combined with an integrated IF processor on the same wafer. To our knowledge, this work represents the first demonstration of a fully integrated millimeter-wave subsystem to date.

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